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1V All-MOS ΣΔ A/D Converters in the Log-Domain

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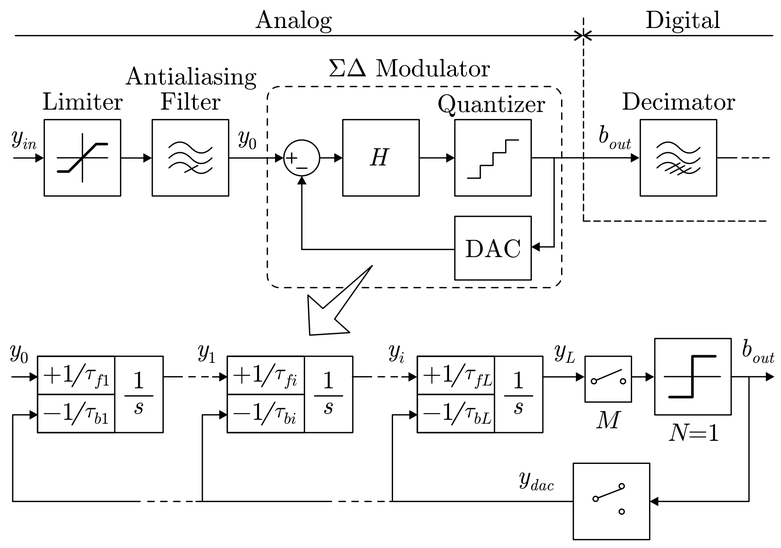
Introduction

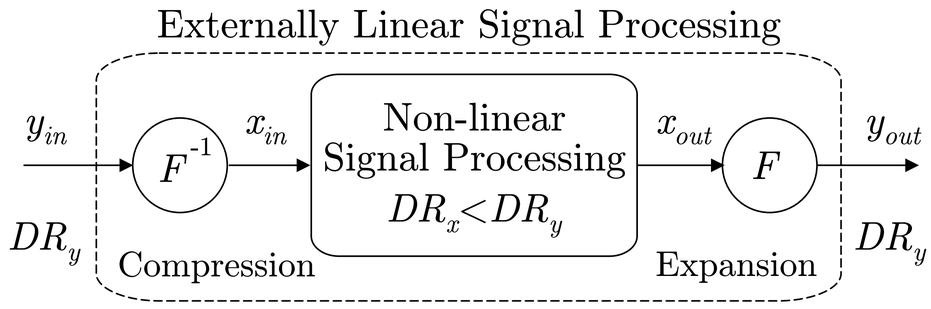
- Oversampling ΣΔ Modulators for A/D Converters



...for very low-voltage (i.e. 1V) and all-MOS SoCs??

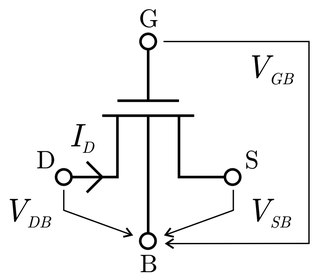
CMOS Log-Domain Proposal

- Log Companding scheme $y = F(x) = e^x$



- The MOSFET operating in subthreshold

for $V_{SB,DB} \gg \frac{V_{GB}-V_{TO}}{n}$ and $V_{DB} - V_{SB} \gg U_t$

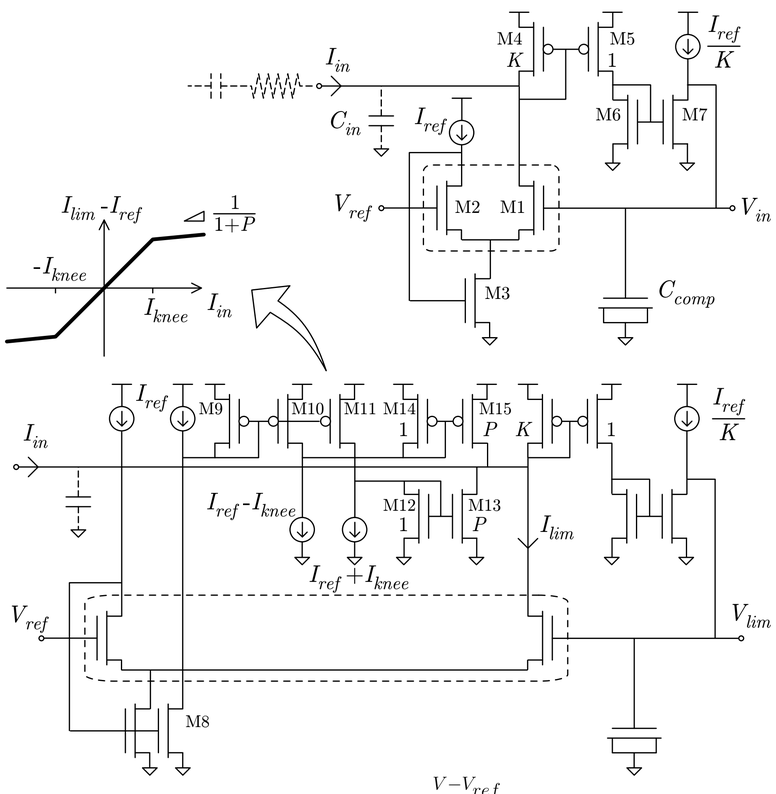


$$I_D = I_S e^{\frac{V_{GB}-V_{TO}}{nU_t}} e^{-\frac{V_{SB}}{U_t}} \qquad I_S = 2n\beta U_t^2$$

$$y_i = \frac{I_{Di}}{I_S} \quad \overset{F}{\underset{}{\longleftrightarrow}} \quad x_i = \frac{V_{GBi}}{nU_t}$$

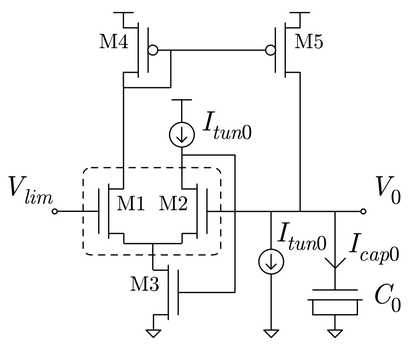
Basic Building Blocks

- Input Compressor and Limiter



$$I = F(V) = I_{ref} e^{\frac{V-V_{ref}}{nU_t}} \quad I > 0$$

- Anti-Alias Filter



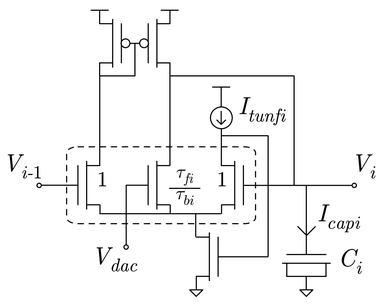
$$\frac{dI_0}{dt} = -2\pi f_c I_0 + 2\pi f_c I_{lim}$$

$$\downarrow$$

$$\underbrace{C_0 \frac{dV_0}{dt}}_{I_{cap0}} = -I_{tun0} + I_{tun0} e^{\frac{V_{in}-V_0}{nU_t}}$$

$$f_c = \frac{1}{2\pi} \frac{I_{tun0}}{nU_t C_0}$$

- Modulator Integrators



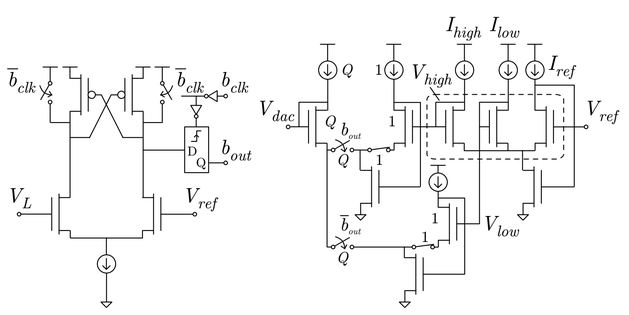
$$\frac{dI_i}{dt} = \frac{1}{\tau_{fi}} I_{i-1} - \frac{1}{\tau_{bi}} I_{dac}$$

$$\downarrow$$

$$\underbrace{C_i \frac{dV_i}{dt}}_{I_{capi}} = I_{tunfi} e^{\frac{-V_i}{nU_t}} \left(e^{\frac{V_{i-1}}{nU_t}} - \frac{\tau_{fi}}{\tau_{bi}} e^{\frac{V_{dac}}{nU_t}} \right)$$

$$\tau_{fi} = \frac{nU_t C_i}{I_{tunfi}}$$

- Modulator Quantizer and DAC



Voltage compression allows:

- Non-linear NMOS capacitors
- True 1V operation

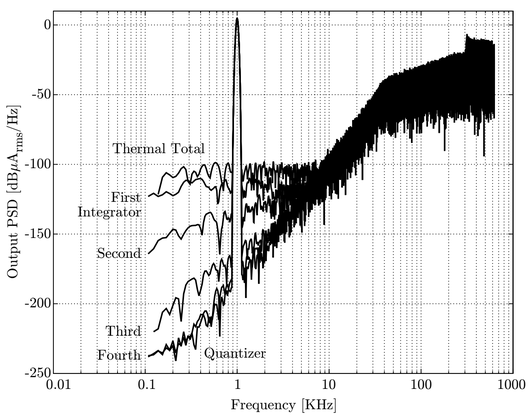
example:

$$\frac{I_{high}}{I_{low}} = \frac{11\mu A}{1\mu A}$$

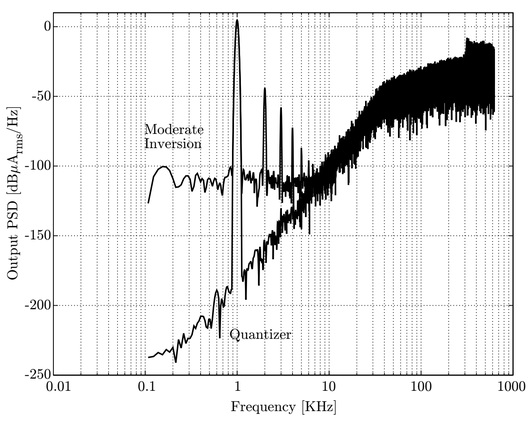
$$(V_{high} - V_{low}) \simeq 3U_t = 75\text{mV}(25^o\text{C})$$

Second-Order Effects

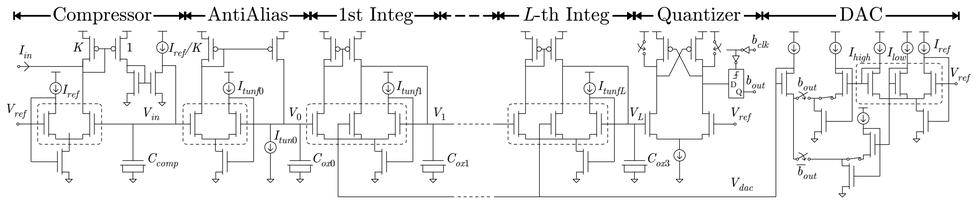
- Thermal noise



- Moderate inversion distortion

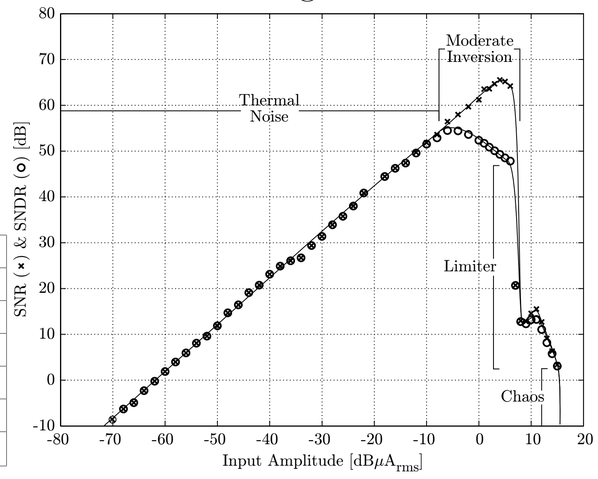


Design Example: 4th-order 1bit 64-oversampling ΣΔ ADCs for Hearing Aids



- Optimal coefficients from literature
- C_{oxi} can be large ($t_{ox} < t_{poly-poly}/5$)
- $I_{tuni} \epsilon [0.5, 6]\mu A \quad C_{oxi} \epsilon [80, 500]$pF
- Experimental ASIC 0.35μm in short

Supply Voltage	1.0	V
Max. $V_{TON}+\lvert V_{TOP}\rvert$	1.3	V
Input Full-Scale	10	μA_{pp}
Input Bandwidth	0.1-8	KHz
Dynamic Range	73	dB
Power Consumption	75	μW
Si Area	<0.5	mm^2



Conclusions

- Log-Domain CMOS ΣΔ ADCs in subthreshold
- Basic building blocks for 1V and sub-100μW
- Fully integration in digital VLSI technologies

References

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[3] F.Serra-Graells, "VLSI CMOS Low-Voltage Log Companding Filters," in *Proceedings of the ISCAS*. IEEE, May 2000, vol. I, pp. 172–175.
[4] F.Serra-Graells, "All-MOS Subthreshold Log Filters," in *Proceedings of the ISCAS*. IEEE, May 2001, vol. I, pp. 137–140.
[5] D.Python, M.Punzenberger, and C.Enz, "A 1-V CMOS Log-Domain Integrator," in *Proceedings of the ISCAS*. IEEE, 1999, vol. II, pp. 685–688.