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All-MOS Subthreshold Log Filters

Francisco Serra-Graells
paco.serra@cnm.es

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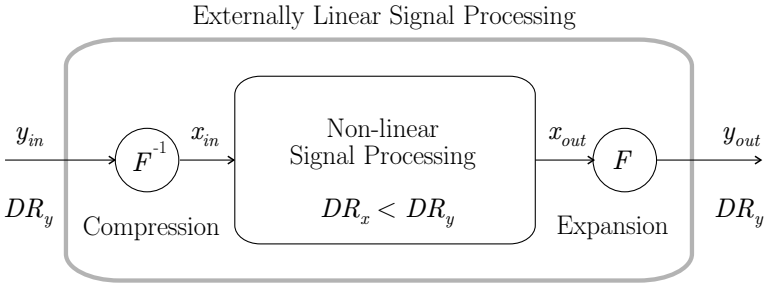
Centro Nacional de Microelectrónica-IMB, Campus UAB, 08193 Bellaterra, Spain

▶ Instantaneous Companding Processing



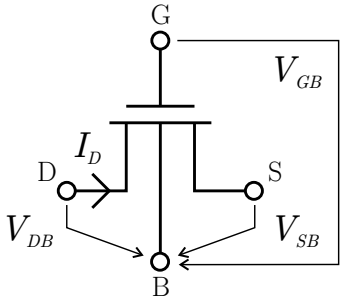
$y \equiv$ Current $\quad x \equiv$ Voltage

▶ Log Companding law: $y = F(x) = e^x$

▶ Application environments:

- High-frequency
- Low-voltage
- **Non-linear capacitive elements?**

▶ Subthreshold MOSFET Implementation



▶ EKV model in weak inversion: $V_{S,DB} > \frac{V_{GB}-V_{TO}}{n}$

$$I_D = I_S e^{\frac{V_{GB}-V_{TO}}{nU_t}} \left(e^{-\frac{V_{SB}}{U_t}} - e^{-\frac{V_{DB}}{U_t}} \right)$$

$$I_S = 2n\beta U_t^2$$

▶ Saturated and non-saturated cells from the author:

- Low-frequency (up to 100KHz)
- Very low-voltage (down to 1V)
- **All-MOS proposal?**

- State-Space description of the filter:

$$\begin{cases} \frac{\mathrm{d}I}{\mathrm{d}t} = AI + BI_{in} \\ I_{out} = CI + DI_{in} \end{cases}$$

$$\frac{\mathrm{d}I_i}{\mathrm{d}t} = \sum_{j=1}^{N} A_{ij} I_j + \sum_{j=1}^{M} B_{ij} I_{inj} \qquad \text{for } i\text{=1 to } N$$

- Gate- (GD) and Source-Driven (SD) Log functions:

$$I = F(V) = \begin{cases} I_S e^{-\frac{V_{TO}+nV_{bias}}{nU_t}} e^{\frac{V}{nU_t}} & \text{GD} \\ I_S e^{\frac{V_{bias}-V_{TO}}{nU_t}} e^{-\frac{V}{U_t}} & \text{SD} \end{cases}$$

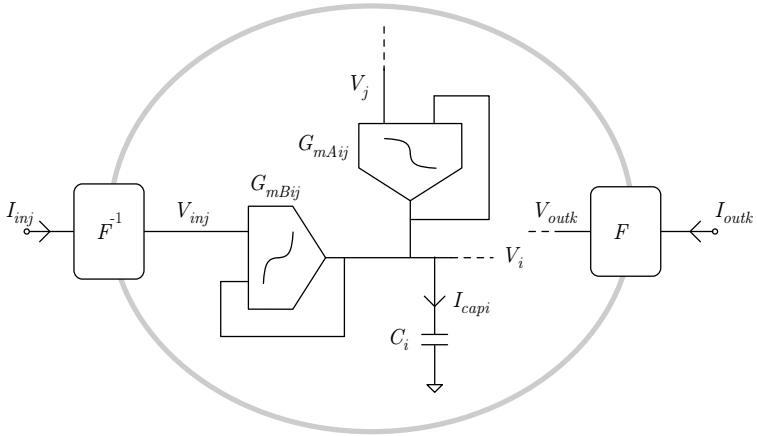
- Equivalent processing in the compressed V-domain:

$$\frac{\mathrm{d}V_i}{\mathrm{d}t} = \begin{cases} \sum_{j=1}^{N} nU_t A_{ij} e^{\frac{V_j - V_i}{nU_t}} + \ldots & \text{GD} \\ -\sum_{j=1}^{N} U_t A_{ij} e^{\frac{V_i - V_j}{U_t}} - \ldots & \text{SD} \end{cases}$$

- Monolithic integration through linear capacitors:

$$\underbrace{C_i \frac{\mathrm{d}V_i}{\mathrm{d}t}}_{I_{capi}} = \begin{cases} \sum_{j=1}^{N} I_{tunAij} e^{\frac{V_j - V_i}{nU_t}} + \ldots & \text{GD} \\ -\sum_{j=1}^{N} I_{tunAij} e^{\frac{V_i - V_j}{U_t}} - \ldots & \text{SD} \end{cases}$$

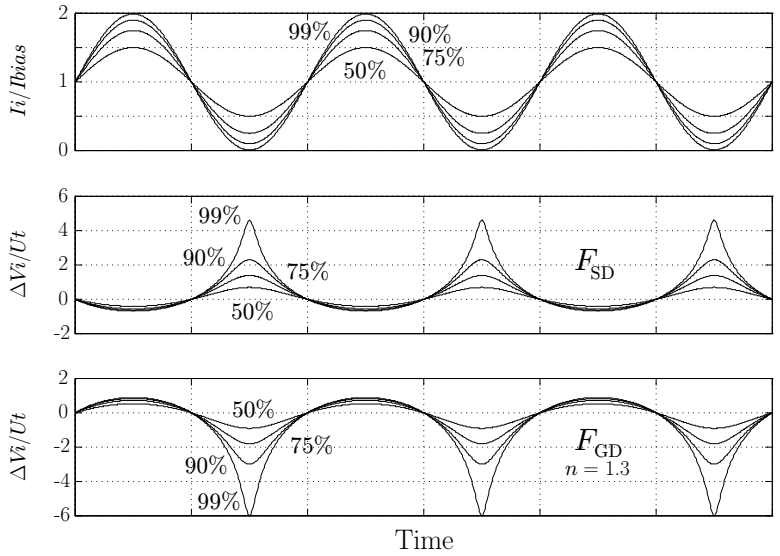
$$I_{tunAij} = \begin{cases} nU_t C_i A_{ij} & \text{GD} \\ U_t C_i A_{ij} & \text{SD} \end{cases}$$



- Actual State-Space variable to be controlled:

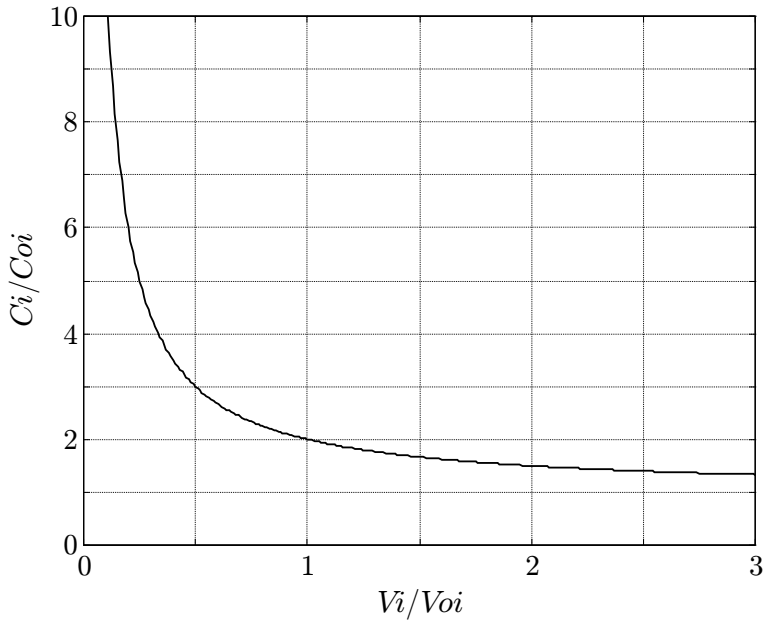
$$I_{capi} = \frac{\mathrm{d}Q_i}{\mathrm{d}t} = C_i\frac{\mathrm{d}V_i}{\mathrm{d}t} + \frac{\mathrm{d}C_i}{\mathrm{d}t}V_i = \underbrace{\left(C_i + \frac{\mathrm{d}C_i}{\mathrm{d}V_i}V_i\right)}\frac{\mathrm{d}V_i}{\mathrm{d}t} \quad \text{versus} \quad C_i\frac{\mathrm{d}V_i}{\mathrm{d}t} = \begin{cases} \sum_{j=1}^{N} I_{tunAij}e^{\frac{V_j - V_i}{nU_t}} + \ldots & \text{GD} \\ -\sum_{j=1}^{N} I_{tunAij}e^{\frac{V_i - V_j}{U_t}} - \ldots & \text{SD} \end{cases}$$

- Causes of signal distortion:
  - Variation of capacitance ($\frac{\mathrm{d}C_i}{\mathrm{d}V_i} \neq 0$)
  - Signal range itself (V_i) $\rightsquigarrow$ Minimized in Log Companding!
- Two general approaches:
  - Capacitance compensation (C_i)
  - Tuning-current compensation (I_{tunAij})



▶ Capacitance Compensation:

$$C_i \doteq C_{oi}\left(1+\frac{V_{oi}}{V_i}\right)$$



$$\left(C_i+\frac{\mathrm{d}C_i}{\mathrm{d}V_i}V_i\right)\equiv C_{oi}\neq f(V_i)$$

Difficult to synthesize in VLSI technologies!

▶ Tuning-Current Compensation:

$$I_{tunAij}=I_{tunoAij}\left(\frac{C_i}{C_{oi}}+\frac{\mathrm{d}C_i}{\mathrm{d}V_i}\frac{V_i}{C_{oi}}\right)$$

$$I_{tunoAij}\doteq\begin{cases} nU_tC_iA_{ij} & \text{GD}\\ U_tC_iA_{ij} & \text{SD}\end{cases}$$

▶ Non-linear re-shaping:

- Depends on the C/V law of the capacitor. . .
- . . . but limited to a window of $< 5U_t$

Available capacitors in digital VLSI technologies?

⇕

The MOSFET itself!

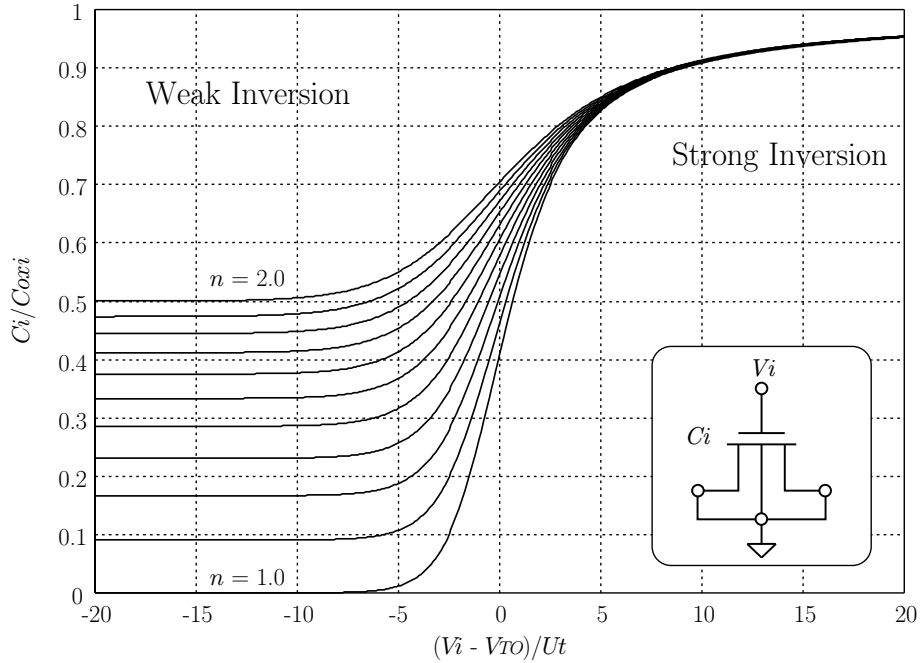
- NMOS capacitor proposal:

$$C_i \doteq C_{GG} \equiv C_{GB} + C_{GS} + C_{GD}$$

- Unified EKV model for all regions of inversion:

$$C_i = C_{oxi}\frac{\frac{n-1}{n}+2\sqrt{IC}\left(1-e^{-\sqrt{IC}}\right)}{1+2\sqrt{IC}\left(1-e^{-\sqrt{IC}}\right)}$$

$$IC = \ln^2\left(1+e^{\frac{V_i-V_{TO}}{2nU_t}}\right)$$



- Flat regions of capacitance:

$$C_i \simeq \begin{cases} \frac{n-1}{n}C_{oxi} & IC \ll 1 \quad \text{deep weak inv.} \\ C_{oxi} & IC \gg 1 \quad \text{deep strong inv.} \end{cases}$$

Sweep of $\pm 20U_t$ around Threshold Voltage

$\Updownarrow$

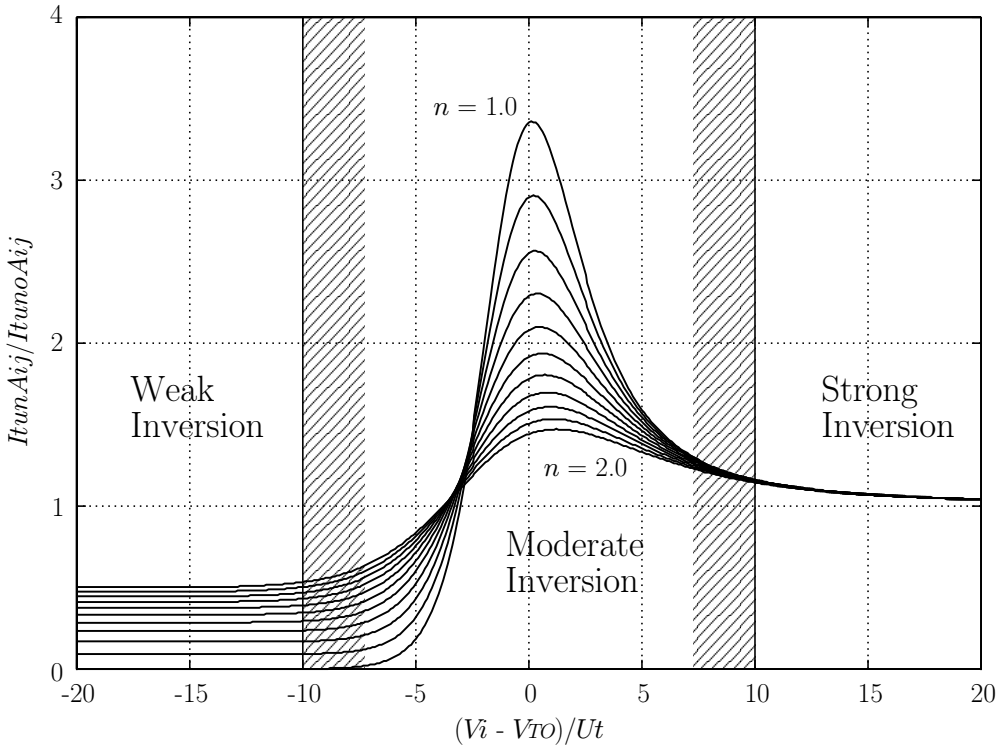
$V_{TO} = 0.5\text{V}$ and $V_{DD} = 1V$ at Room Temperature

- Tuning-current compensation for NMOS capacitance:

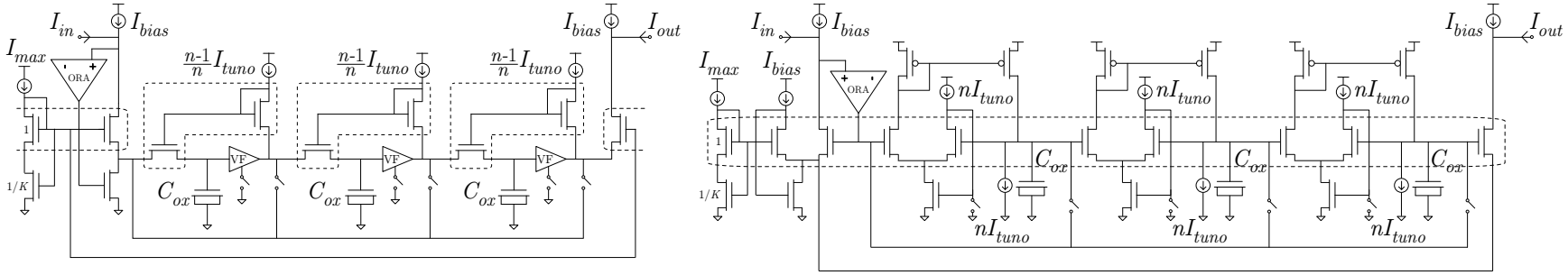
$$I_{tunAij} \simeq \begin{cases} \frac{n-1}{n} I_{tunoAij} & IC \ll 1 \\ I_{tunoAij} & IC \gg 1 \end{cases}$$

- Topological compatibility with GD and SD Log functions:

$$I_{tunAij} \simeq \begin{cases} \frac{n-1}{n} U_t C_{oxi} A_{ij} & \text{SD} \\ n U_t C_{oxi} A_{ij} & \text{GD} \end{cases}$$



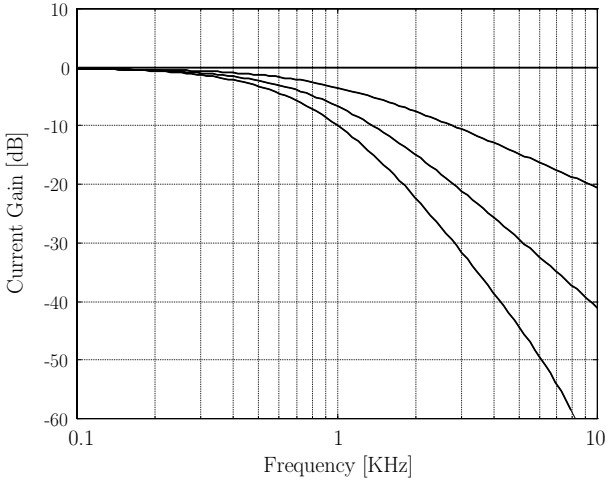
- Third-order cascaded filter:



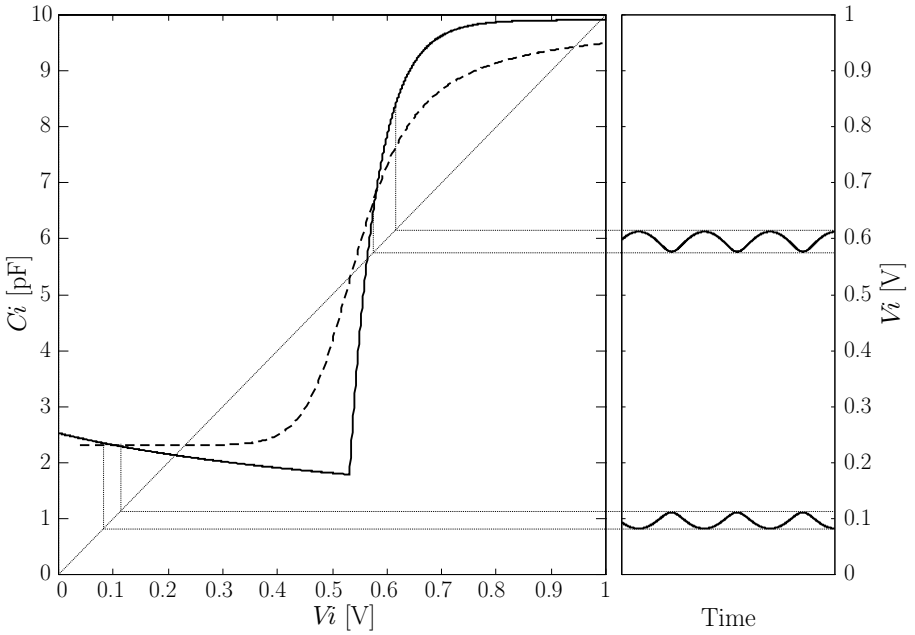
$$I_{tuno} = U_t C_{ox} 2\pi f_c$$

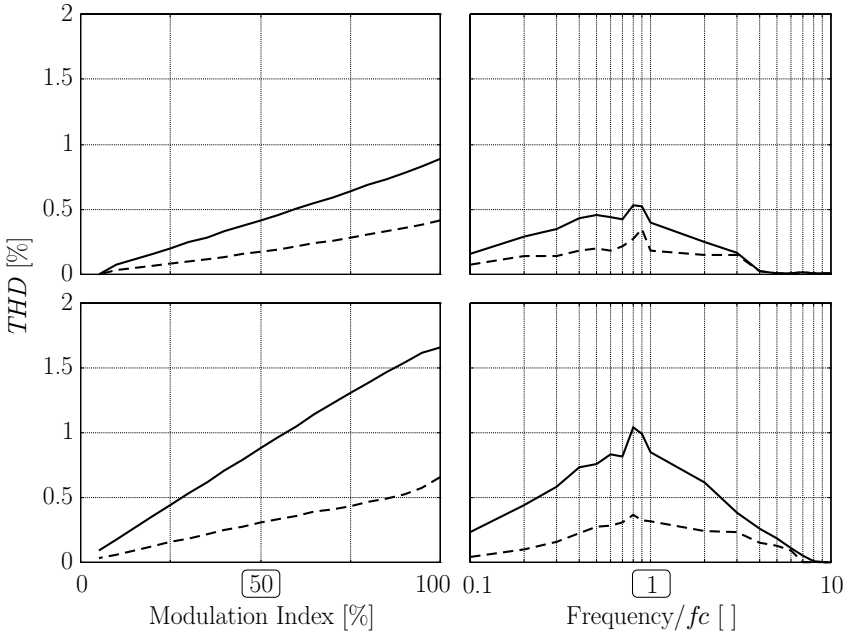
- Common circuit specifications:

Parameter	Value	Units
Supply Voltage	1.0	V
$(V_{TON} + \|V_{TOP}\|)max$	1.3	V
Full-Scale (I_{max})	4	μA_{pp}
Corner Frequencies @-3dB (f_c)	500-5000	Hz
Oxide Capacitance per Pole (C_{ox})	10	pF
Tuning Currents (I_{tuno})	1-10	nA
Technology	1.2	μm



First to third order selection





Example for $K = 10$

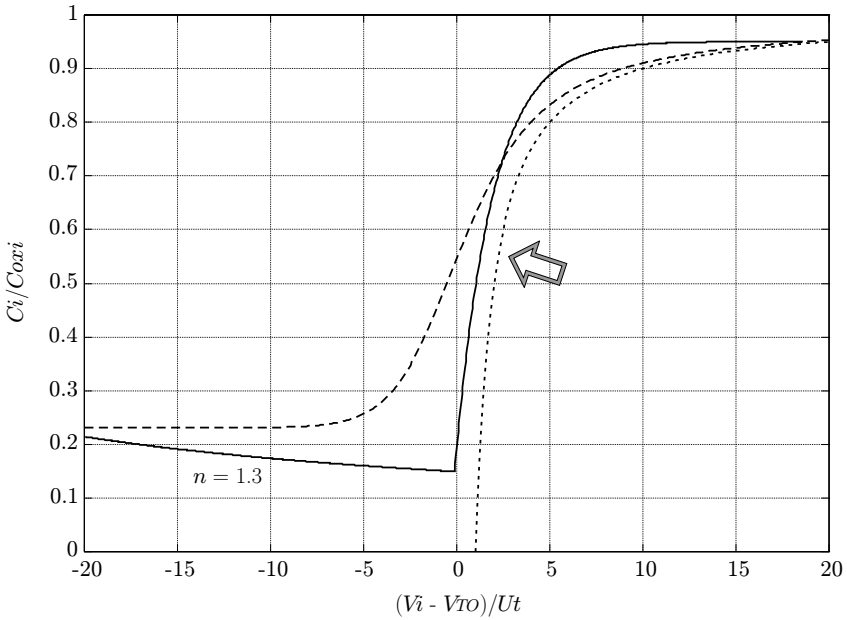
- 1V supply voltage
- Third-order selection

Design of the compressed operating point in the V-domain

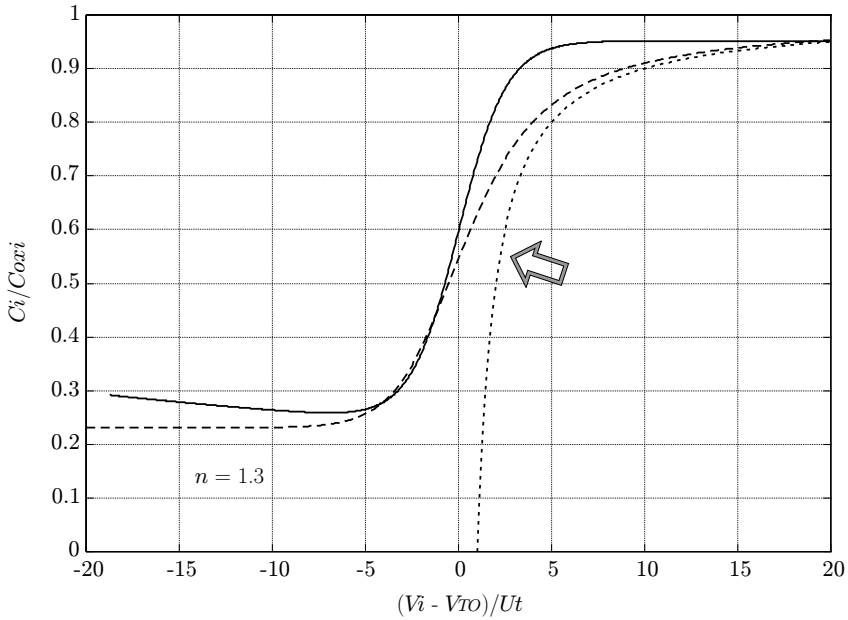
$\updownarrow$

External linearity in the I-domain

- MOS-Capacitance Model Requirements:



BSIM1 for a 1.2μm VLSI technology



BSIM3 for a 0.35μm VLSI technology

- Currently working on an analytical approximation of C_i for GD cells

▶ Si Area Savings or Dynamic Range Improvements:

Parameter	Process A	Process B	Units
λ	1.2	0.35	μm
t_{oxgate}	18.5	7.5	nm
C_{gate}	1.87	4.6	fF/μm^2
t_{oxpoly}	50	40	nm
C_{poly}	0.69	0.86	fF/μm^2
C_{gate}/C_{poly}	2.7	**5.4**	-

▶ Constant Power:

$$A_{gate} < \frac{A_{poly}}{5} \qquad I_{tungate} \equiv I_{tunpoly}$$

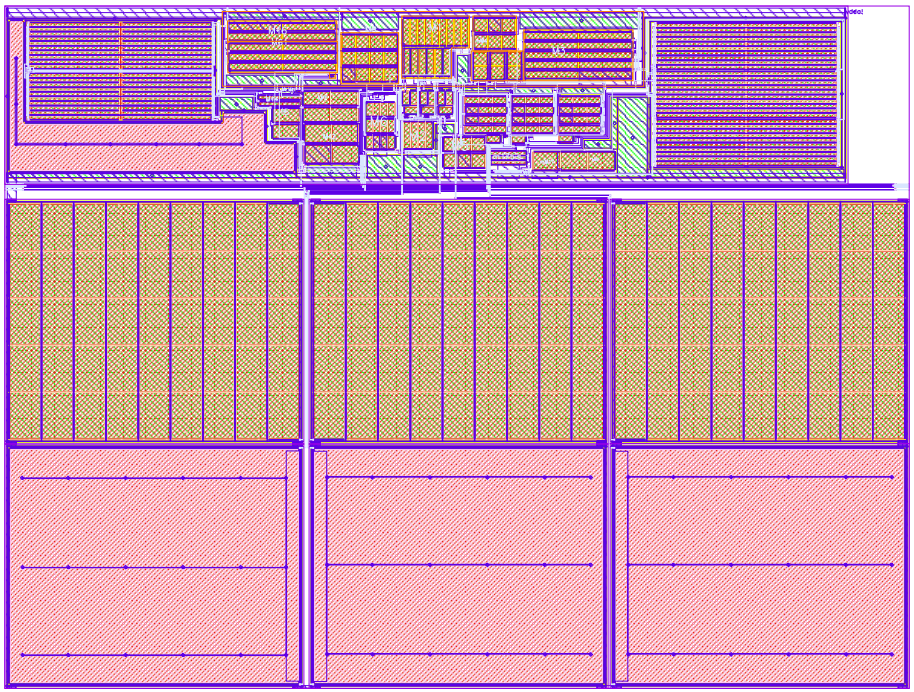
▶ Constant Si Area:

$$A_{gate} \equiv A_{poly} \qquad I_{tungate} > 5 I_{tunpoly}$$

$$SNR_{thermal} \propto 20 \log \sqrt{I_{tun}}$$

$$DR_{gate} > DR_{poly} + 7\text{dB}(1\text{bit})$$

A dual third-order low-pass GD filter



$C_{poly} = 45\text{pF}$ $C_{gate} = 243\text{pF!!}$

- Non-linear capacitance $\equiv$ local tuning-current compensation
- NMOS capacitors compatible with existing CMOS cells
- Distortion strongly related to compressed operating point
- Important Si area savings or Dynamic Range improvements
- Suitable for 1V analog circuits in digital VLSI technologies