ESSCIRC 2001: 27th European Solid-State Circuits Conference, Villach, Austria, Sep 2001

A True 1V CMOS Log-Domain Analog Hearing-Aid-on-a-Chip

Francisco Serra-Graells[1](paco.serra@cnm.es), Lluís Gómez[2](llgomez@gaes.es) and Òscar Farrés[1](oscar.farres@cnm.es)
[1] cnm (Centro Nacional de Microelectrónica, Spain) [2] GAES-MICROSON (Microson S.A., Spain)

Design Problem

Very Low-Voltage (down to 1V) CMOS Systems-on-a-Chip

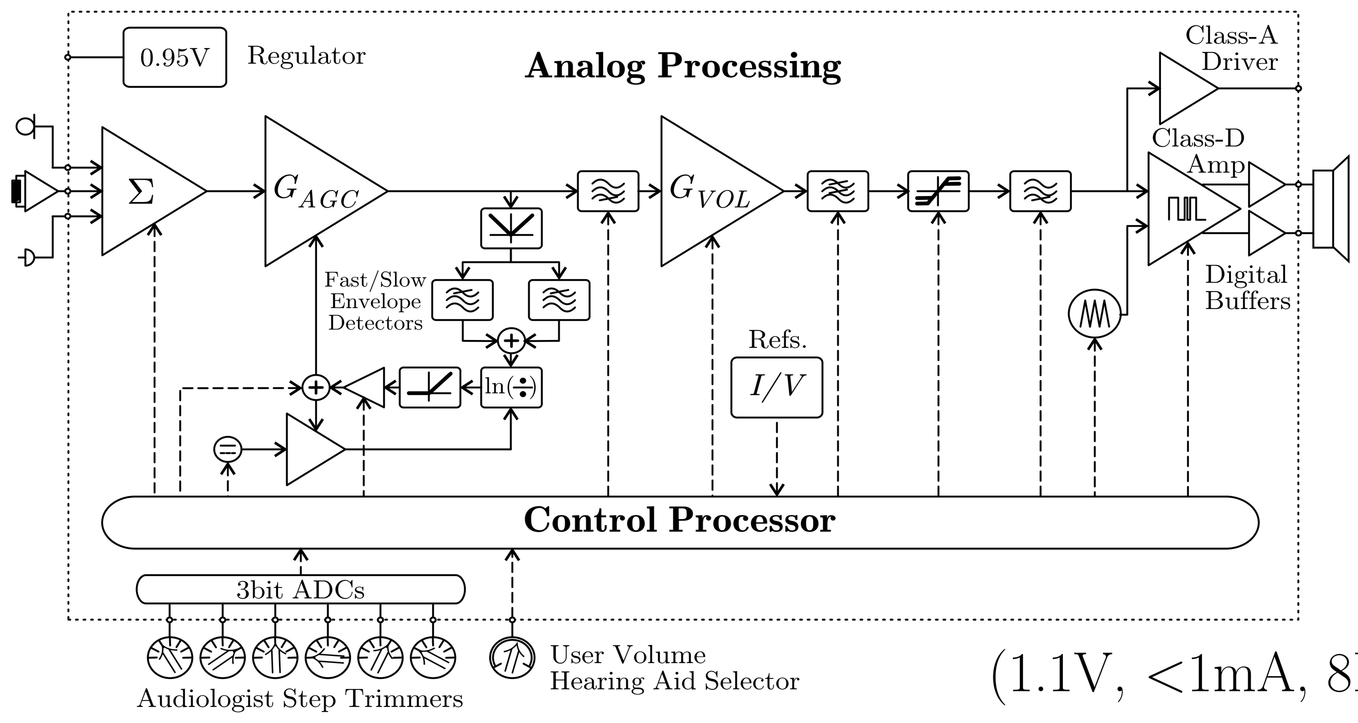
↓ Battery Technology

Analog design problem typically approached using Charge-Pump based Supply Multipliers...

↓

Extra power+area+components!

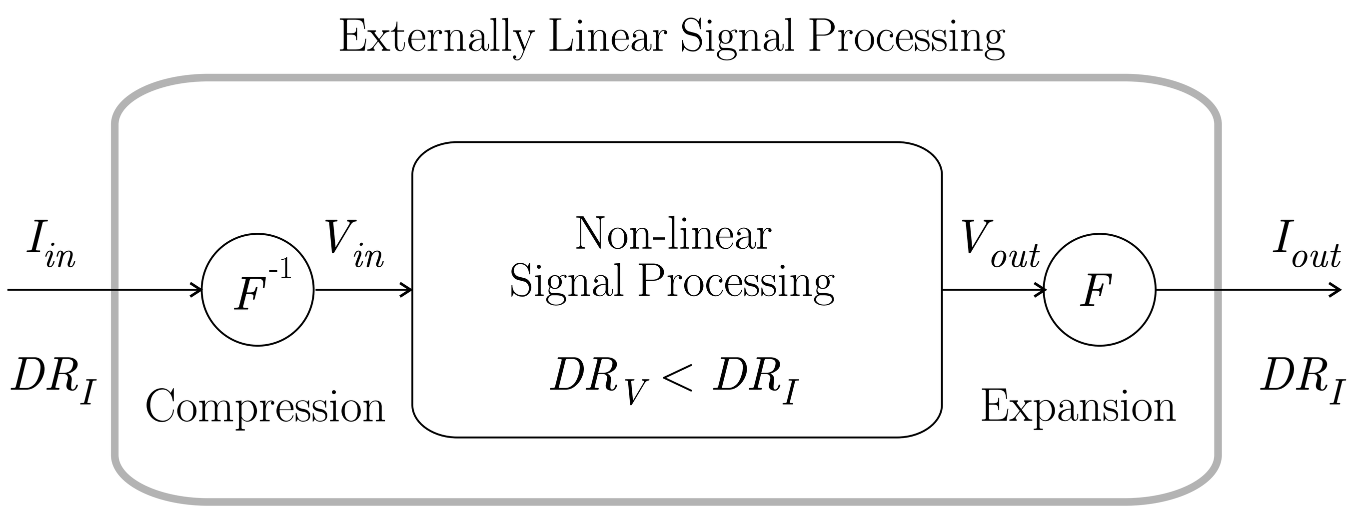
Application Example: Analog Hearing-Aids



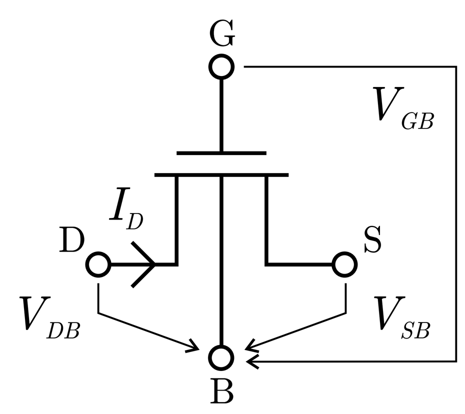
(1.1V, <1mA, 8KHz)

Novel Analog CMOS Circuit Technique

Log Companding Theory $I = F(V) = K_1 e^{K_2 V}$



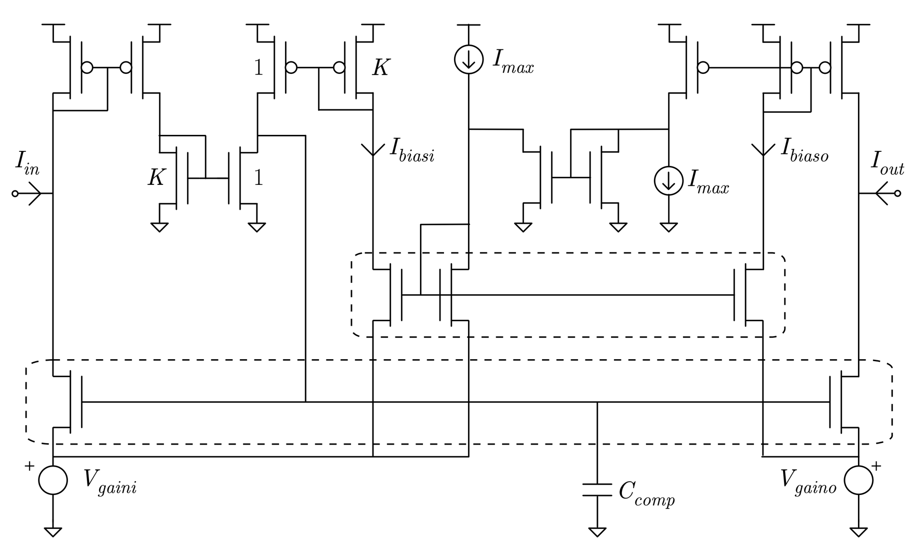
MOSFET Operating in Subthreshold



$$I = F(V) = \begin{cases} I_S e^{-\frac{V_{TO}+nV_{bias}}{nU_t}} e^{\frac{V}{nU_t}} & \text{GD} \\ I_S e^{\frac{V_{bias}-V_{TO}}{nU_t}} e^{-\frac{V}{U_t}} & \text{SD} \end{cases}$$

↘ ↙

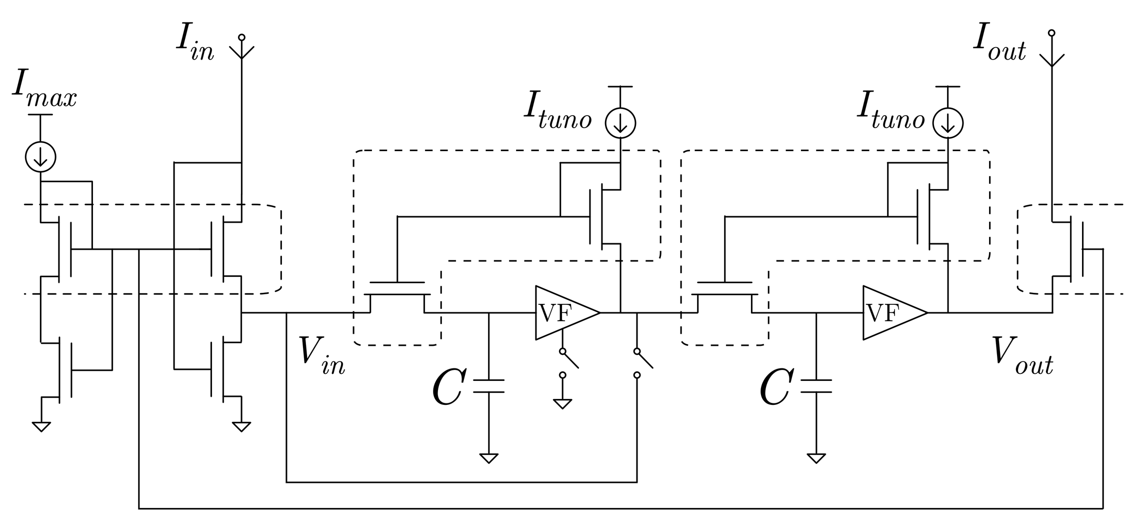
• Amplification



$$G[\text{dB}] = 20\log(e)\frac{V_{gaini}-V_{gaino}}{U_t} \qquad \zeta = \frac{1}{2}\sqrt{\frac{KC_{comp}}{C_{in}}}$$

Tuning: ±40dB, 0.43dB/mV(25°C) and suitable for AGC

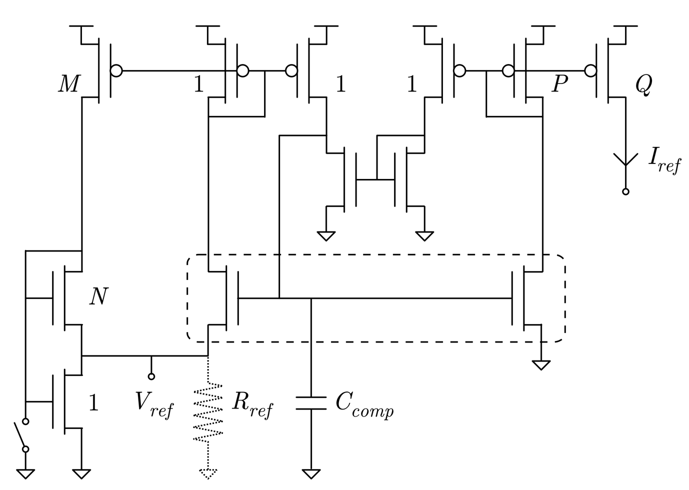
• Filtering



$$f_{-3\text{dB/stage}} = \frac{I_{tuno}}{2\pi U_t C}$$

Tuning: 0.64KHzpF/nA(25°C) and programmable order

• Generation

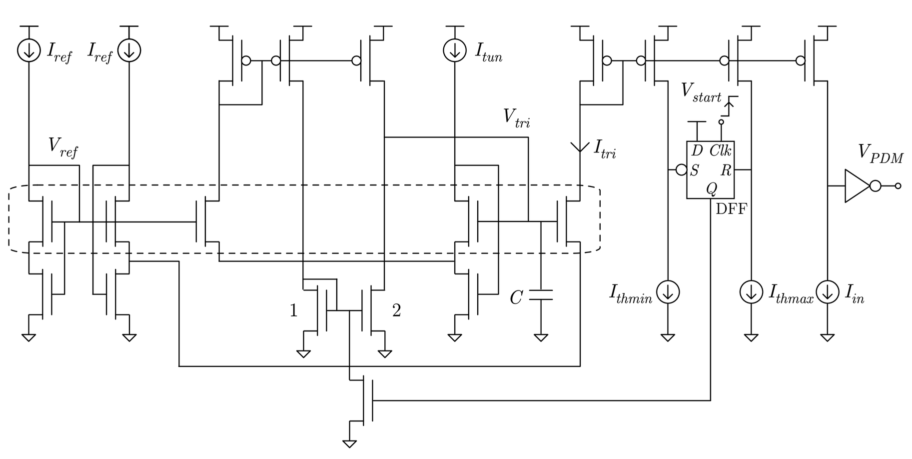


$$V_{ref} = U_t \ln P$$

$$I_{ref} = \begin{cases} Q\frac{U_t}{R_{ref}}\ln P & \text{on} \\ Q\left[\frac{\ln P}{2(M+1)}\left(\sqrt{\frac{M}{N}}+\sqrt{\frac{M}{N}+M+1}\right)\right]^2 I_S & \text{off} \end{cases}$$

PTAT References for Gain and Corner Frequency

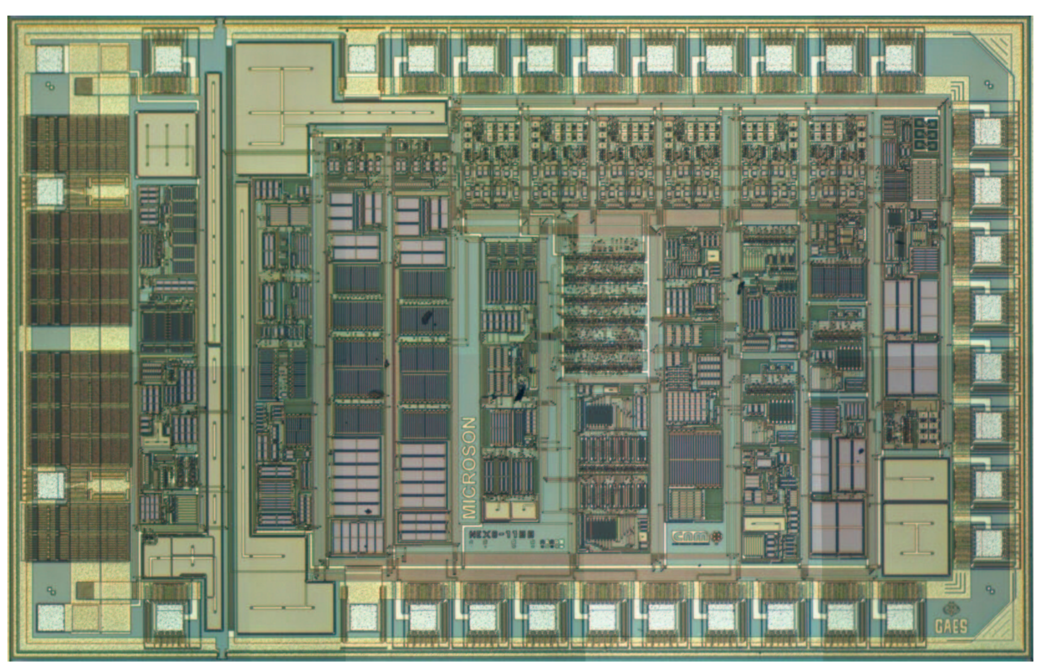
• Pulse Duration Modulation



$$T = \frac{2(I_{thmax}-I_{thmin})nU_tC}{I_{tuno}}$$

Low-Offset and Multi-Frequency PDM

Product Example: NEXO (A True 1V CMOS Analog Hearing-Aid-on-a-Chip)



Actual size: ▪ 1mm

Parameter		This design	[1]	[2]	Units
HA models		BTE,ITE ITC,CIC	CIC	BTE,ITE ITC,CIC	
Technology		CMOS	Bipolar	CMOS	
V_{DDmin}		1.0	1.1	1.1(×2)	V
I_{DDQ} @R_{load}	$\gg$100Ω	0.3	0.4 +	1.1	mA
	$\ll$100Ω	< 0.5	Ext.Class-D	< 1.4	mA
G_{max}		70	48	58	dB
V_{nieq}		6	3	7	μV_{rms}
THD	Class-D	< 1	–	5	%
	Ext.Class-D	0.1	0.6	–	%

- 1.2μm $(V_{TON}+|V_{TOP}|)_{max} = 1.3$V 2P 2M VLSI CMOS technology
- approx. 5K MOSFETs
- $SNR \geq 70$dB (100Hz−10KHz)

Conclusions

The new circuit technique allows:

- Very Low-Voltage operation
- Best power supply saving
- First HA without Supply Multiplier
- Application to ΣΔ Audio ADCs

[1] Gennum Corp. *GA3201 Programmable DynamEQ II: Preliminary Datasheet*, Sep 1999, http://www.gennum.com
[2] Siemens Audiologische Technik GmbH *Music: Technical Information*, 2001, http://www.hoergerate-siemens.com