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VLSI CMOS Low-Voltage Log-Companding Filters

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Abstract

- Introduction
- Principle of Operation and CMOS Generalization
- Basic Building Blocks
- Design Methodology
- Examples
- Conclusions

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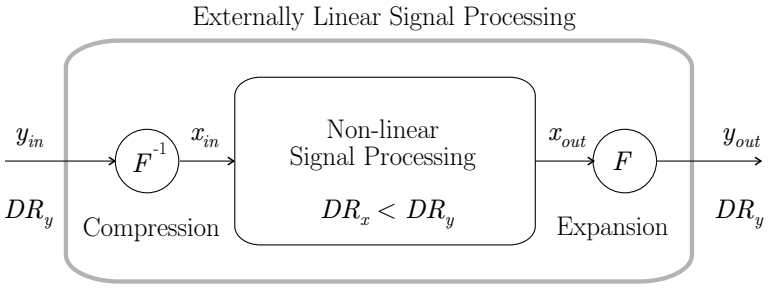
▶ Instantaneous Companding Processing

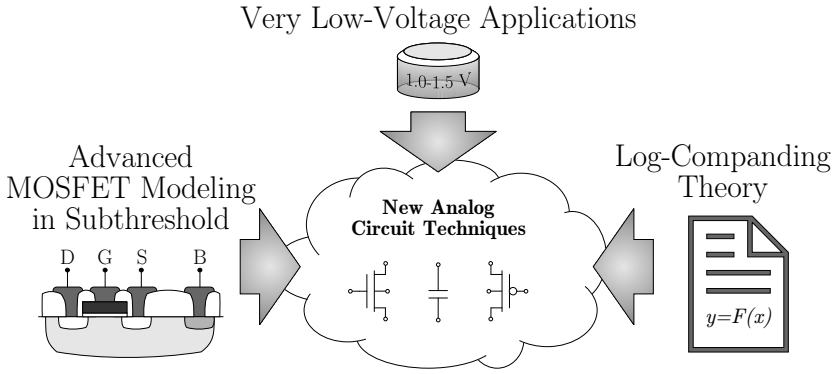


$y \equiv$ Current $\quad x \equiv$ Voltage

High-Frequency & Low-Voltage Applications

- Log-Companding law: $y = F(x) = e^x$
- Previous work mainly in bipolar [1] vs MOS:
  - Asymmetric I/V curves
  - Reduced e^x current dynamic range
  - Poor output conductance
  - Physical mismatching
  - Flicker noise
- Few CMOS realizations [2] [3] [4] [5]

▶ New Proposal



- EKV model [6] in weak inversion: $V_{S,DB} > \frac{V_{GB}-V_{TO}}{n}$

$$I_D = I_S e^{\frac{V_{GB}-V_{TO}}{nU_t}} \left(e^{-\frac{V_{SB}}{U_t}} - e^{-\frac{V_{DB}}{U_t}} \right)$$

$$I_S = 2n\beta U_t^2$$

- Basic Integrator:

$$\frac{\mathrm{d}y_{out}}{\mathrm{d}t} \doteq \frac{y_{in}}{\tau}$$

- Chain Rule as proposed by [7]:

$$\frac{\mathrm{d}y_{out}}{\mathrm{d}t} = \frac{\mathrm{d}y_{out}}{\mathrm{d}x_{out}}\frac{\mathrm{d}x_{out}}{\mathrm{d}x_{cap}}\frac{\mathrm{d}x_{cap}}{\mathrm{d}t} = y_{out}\frac{\mathrm{d}x_{cap}}{\mathrm{d}t}$$

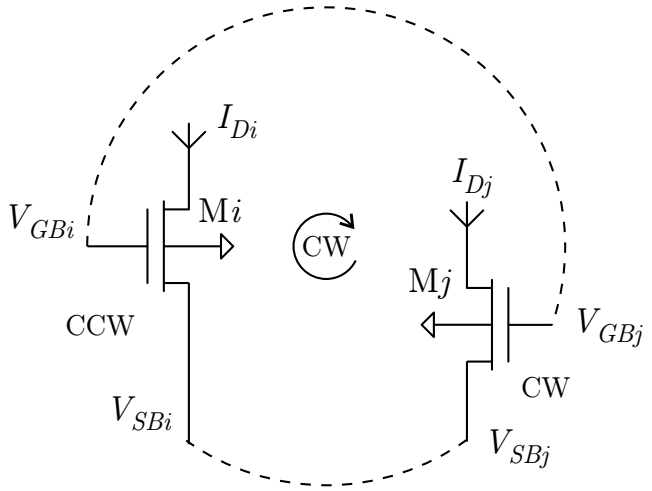
- Product of currents as defined by [8]:

$$y_{out}\underbrace{C\frac{\mathrm{d}x_{cap}}{\mathrm{d}t}} = y_{tun}y_{in} \qquad y_{tun} \doteq \frac{C}{\tau}$$

- Multipliers $\rightsquigarrow$ the Translinear Principle [9]:

$$y_{out}y_{cap} = y_{tun}y_{in}$$

- CMOS Translinear Loops?



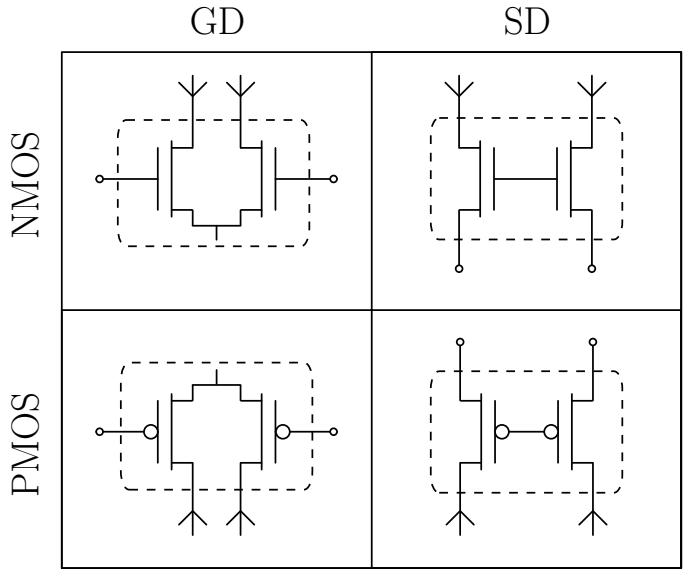
$$\sum_{\mathrm{CCW}} (V_{GB} - V_{SB})_i = \sum_{\mathrm{CW}} (V_{GB} - V_{SB})_j$$

- Cancellation of signal dependent terms:

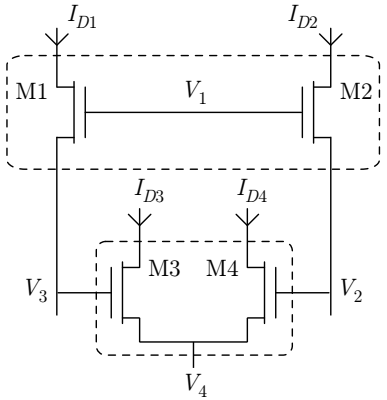
$$\sum_{\text{CCW}} n_i U_t \ln\frac{I_{Di}}{I_{Si}} + V_{TOi} + \underbrace{(n_i-1)V_{SBi}} = \sum_{\text{CW}} n_j U_t \ln\frac{I_{Dj}}{I_{Sj}} + V_{TOj} + \underbrace{(n_j-1)V_{SBj}}$$

$$\sum_{\text{CCW}} U_t \ln\frac{I_{Di}}{I_{Si}} + \frac{V_{TOi}}{n_i} + \underbrace{(1-\frac{1}{n_i})V_{GBi}} = \sum_{\text{CW}} U_t \ln\frac{I_{Dj}}{I_{Sj}} + \frac{V_{TOj}}{n_j} + \underbrace{(1-\frac{1}{n_j})V_{GBj}}$$

- Gate/Source Driven (G/SD) matched pairs



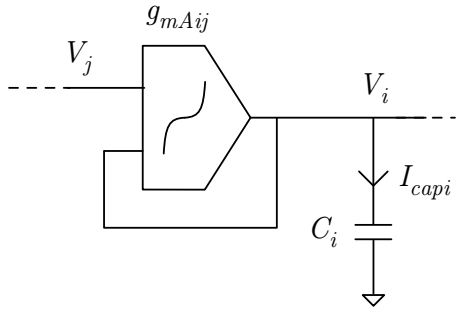
- No GD/SD mixing!



$$\frac{I_{D1}}{I_S}\left(\frac{I_{D3}}{I_S}\right)^{n3} = \frac{I_{D2}}{I_S}\left(\frac{I_{D4}}{I_S}\right)^{n4}$$

- Rewriting the product for systematic synthesis:

$$C\frac{\mathrm{d}x_{out}}{\mathrm{d}t} = y_{tun}e^{x_{in}-x_{out}}$$



- State-Space matrix description:

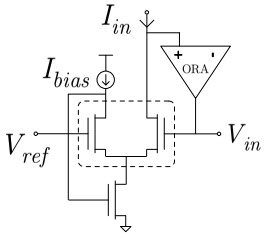
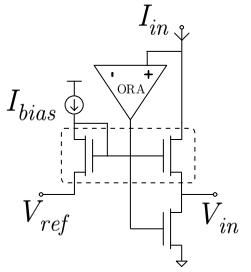
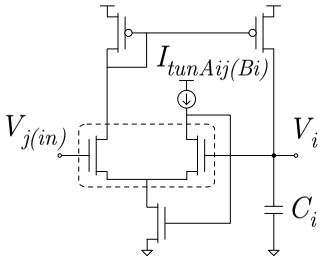
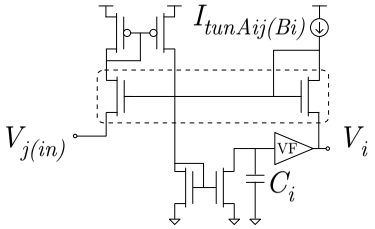
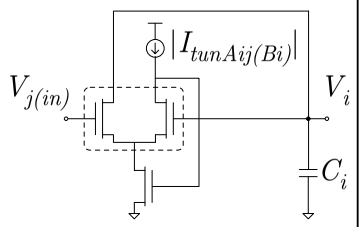
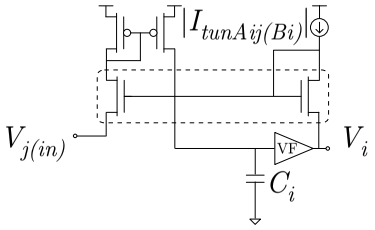
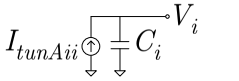
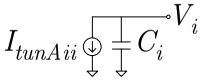
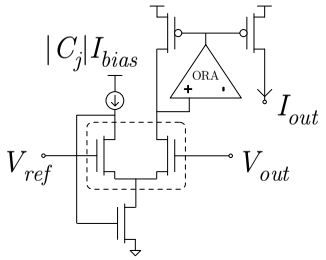
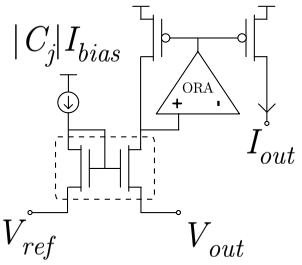
$$\begin{cases} \frac{\mathrm{d}I}{\mathrm{d}t} = AI + BI_{in} \\ I_{out} = CI + DI_{in} \end{cases}$$

- Proposed CMOS Log-Companding functions:

$$I = F(V) = \begin{cases} I_S e^{-\frac{V_{TO}+nV_{ref}}{nU_t}} e^{\frac{V}{nU_t}} & \text{GD} \\ I_S e^{\frac{V_{ref}-V_{TO}}{nU_t}} e^{-\frac{V}{U_t}} & \text{SD} \end{cases}$$

$$\frac{\mathrm{d}I_i}{\mathrm{d}t} = \sum_{j=1}^{N} A_{ij}I_j + \sum_{j=1}^{M} B_{ij}I_{inj} \quad \Rightarrow \quad C_i\frac{\mathrm{d}V_i}{\mathrm{d}t} = \begin{cases} \sum_{j=1}^{N} I_{tunAij}e^{\frac{V_j-V_i}{nU_t}} + \sum_{j=1}^{M} I_{tunBij}e^{\frac{V_{inj}-V_i}{nU_t}} & \text{GD} \\ \sum_{j=1}^{N} -I_{tunAij}e^{\frac{V_i-V_j}{U_t}} - \sum_{j=1}^{M} I_{tunBij}e^{\frac{V_i-V_{inj}}{U_t}} & \text{SD} \end{cases}$$

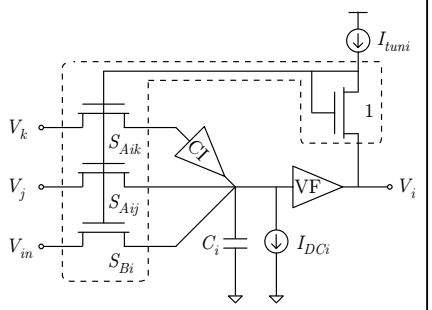
▶ Low-Voltage Saturated CMOS cells:

$I_{tunAij(Bi)}$	GD $nU_tC_iA_{ij}(B_i)$	SD $U_tC_iA_{ij}(B_i)$
Compressor		
$A_{ij}(B_i) > 0$		
$A_{ij}(B_i) < 0$		
A_{ii}		
Expander		

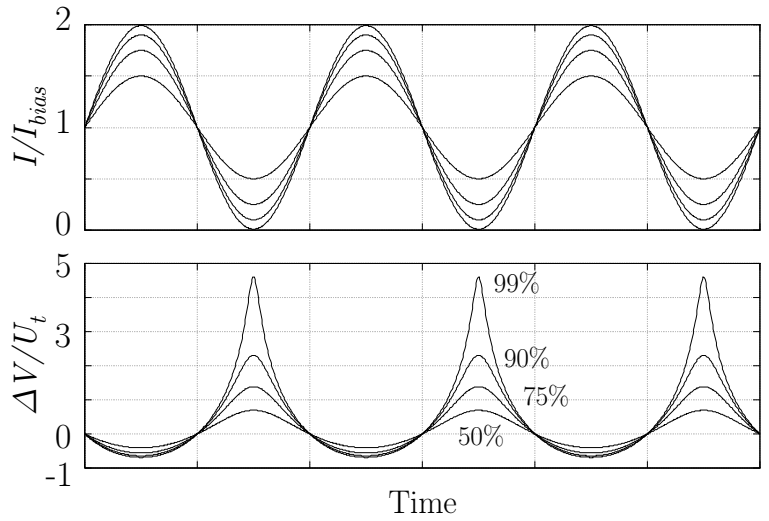
- Low-Voltage Non-Saturated CMOS cells:

- Same Log-Companding F as Saturated SD case, but for A and B:

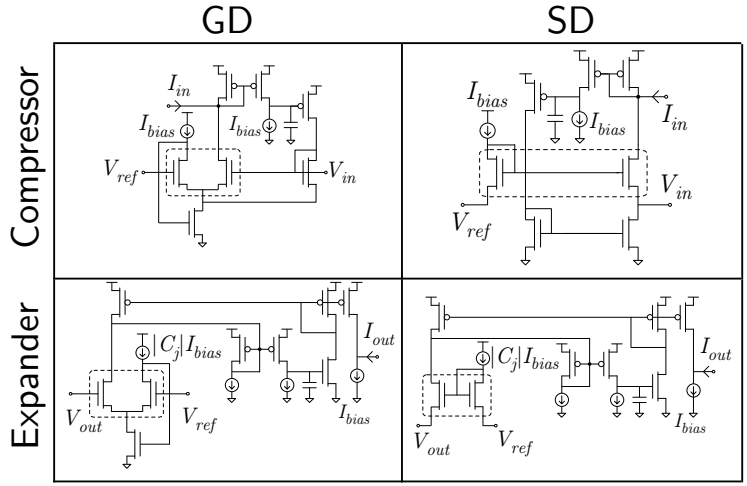
$$C_i\frac{\mathrm{d}V_i}{\mathrm{d}t} = \sum_{j=1}^{N} -I_{tunAij}e^{\frac{V_i-V_j}{U_t}} + \cdots \equiv \sum_{\substack{j=1\\ j\neq i}}^{N} I_{tunAij}e^{\frac{V_i}{U_t}}\underbrace{\left(e^{\frac{-V_i}{U_t}} - e^{\frac{-V_j}{U_t}}\right)} - \sum_{j=1}^{N} I_{tunAij} + \cdots$$

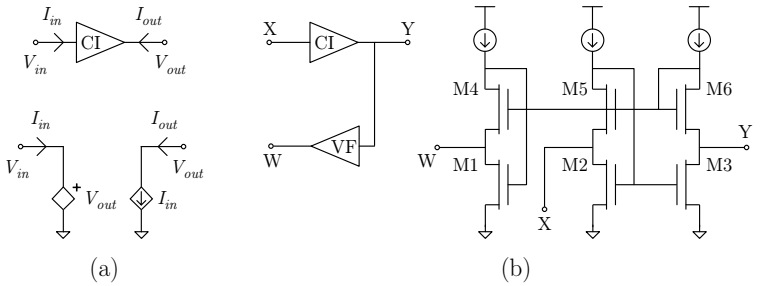
I_{tuni}	$\lvert A_{ii}\rvert U_t C_i$
$A_{ij}(B_i) > 0$ $A_{ik} < 0$	
$S_{Aij(Bi)}$	$\left\lvert\frac{A_{ij}(B_i)}{A_{ii}}\right\rvert$
I_{DCi}	$I_{tuni}\frac{\sum_{j=1}^{N} A_{ij} + B_i}{\lvert A_{ii}\rvert}$

- Signal Boundaries:



▶ Low-Voltage Auxiliary Circuitry:





▶ Comparison:

- Saturated GD $\rightsquigarrow$ area saving
- Saturated SD $\rightsquigarrow$ technology independence & relaxed matching
- Non-Saturated SD $\rightsquigarrow$ idem Saturated SD & low DC errors

- Matrix Procedure A_0, B_0 and C_0 ($D_0 \equiv 0$):

1 Normalize C_0 to share comp/expanders, and $Y_{out}(DC) \equiv Y(DC)$:

$$C_0 M_{norm}^{-1} \doteq I$$

2 Achieve $Y(DC) \equiv Y_{in}(DC)$ keeping previous C_1:

$$C_1 = M_{op} C_1$$

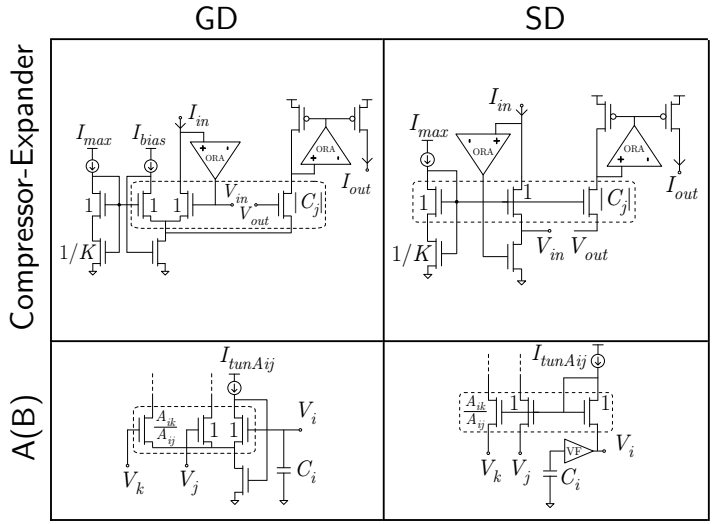
$$\bar{1}_{order} = -M_{op} A_1^{-1} B_1 \bar{1}_{inputs}$$

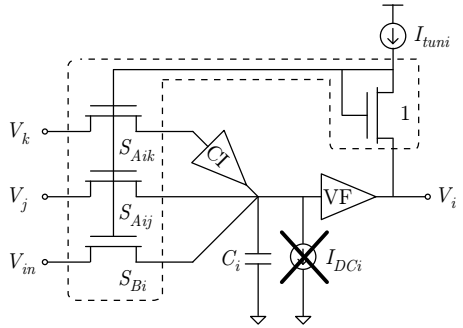
3 If $\nexists M_{op}$, then use an extra dummy input:

$$\bar{0}_{order} = A_1 \bar{1}_{order} + B_1 \bar{1}_{inputs} + \bar{B}_{dummy}$$

$$B_2 = \left[B_1 | \bar{B}_{dummy} \right]$$

- Circuit reductions:

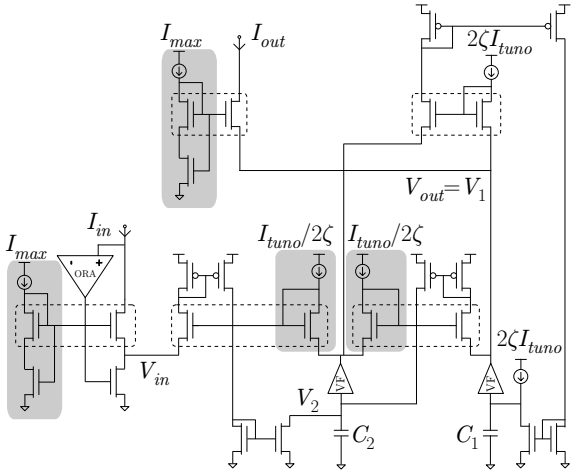




- Synthesis example: SD Saturated 2nd-Order Low-Pass

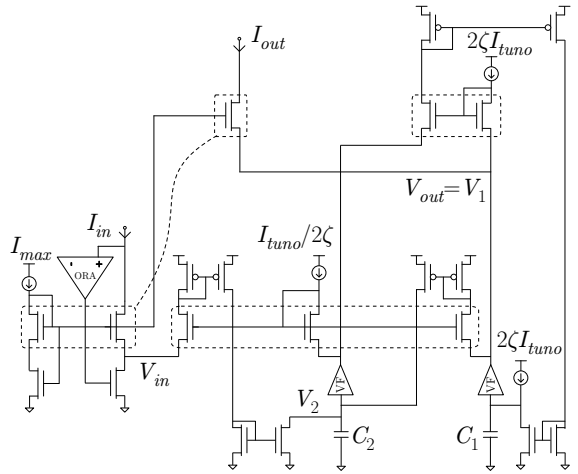
$$A = \begin{bmatrix} -2\zeta w_o & -w_o \\ w_o & 0 \end{bmatrix} \quad B = \begin{bmatrix} 0 \\ -w_o \end{bmatrix} \leftarrow$$

$$C = \begin{bmatrix} 1 & 0 \end{bmatrix} \quad D = \begin{bmatrix} 0 \end{bmatrix}$$



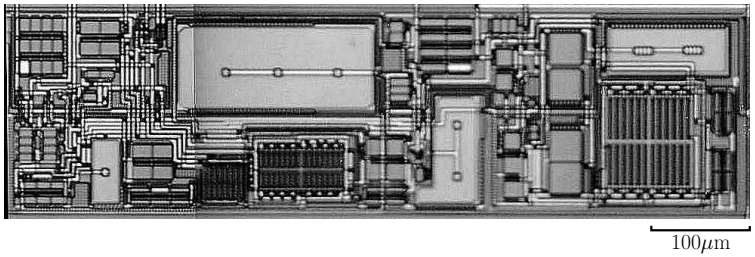
$$A_{new} = \begin{bmatrix} -2\zeta w_o & 2\zeta w_o \\ -\dfrac{w_o}{2\zeta} & 0 \end{bmatrix} \quad B_{new} = \begin{bmatrix} 0 \\ \dfrac{w_o}{2\zeta} \end{bmatrix}$$

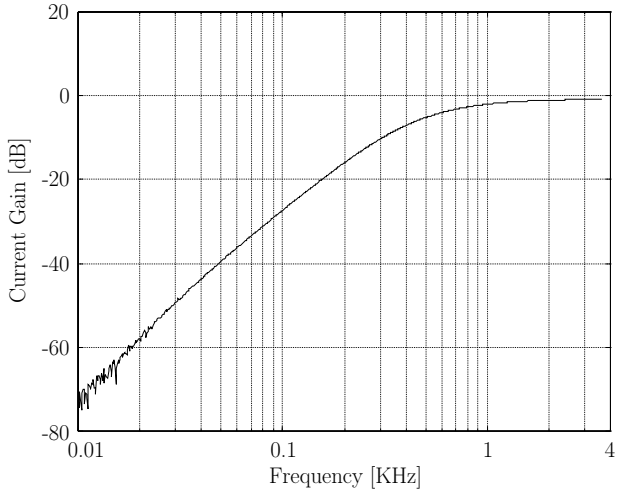
$$C_{new} = \begin{bmatrix} 1 & 0 \end{bmatrix} \quad D_{new} = \begin{bmatrix} 0 \end{bmatrix}$$

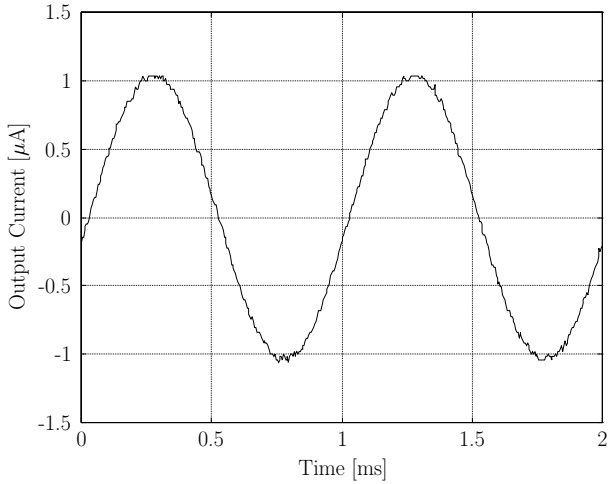


- Common specs:
  - Audio Applications (e.g. Hearing Aids)
  - $V_{DDmin} = 1.0$V
  - $(V_{TON} + |V_{TOP}|)max = 1.25$V
  - $I_{Full-Scale} = 4\mu A_{pp}$
  - THD <1% at 90% Full-Scale
  - DR =60dB to 70dB
  - 10pF< C <100pF
  - 1.2μm VLSI CMOS 2M 2P

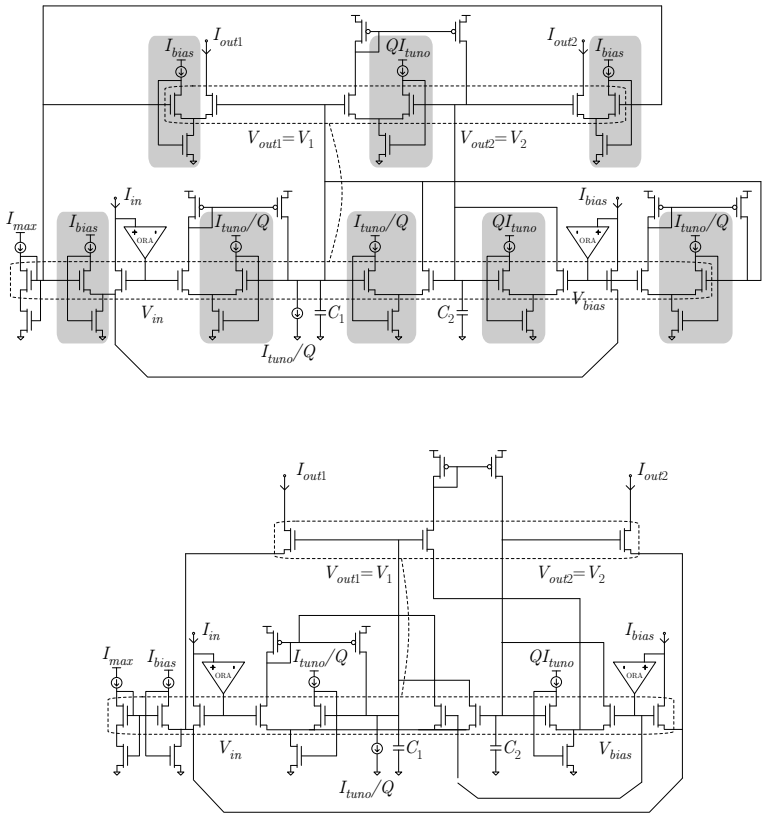
- Saturated SD 2nd-Order High-Pass:

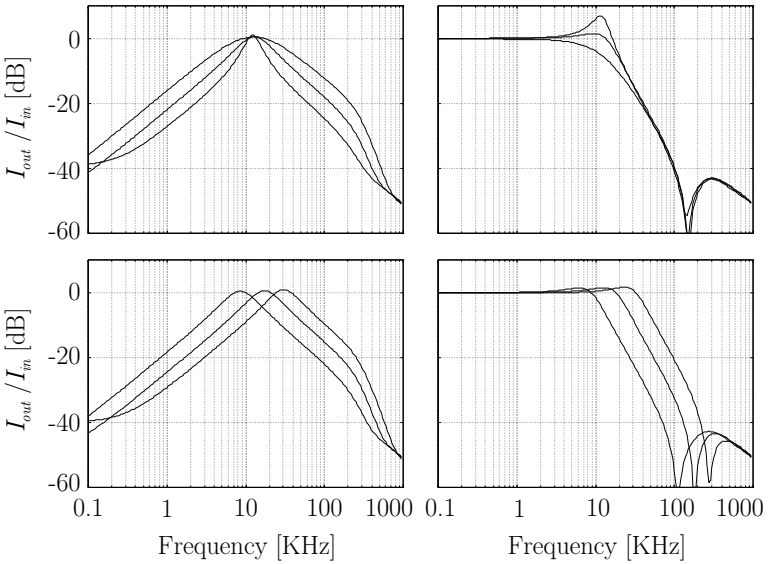




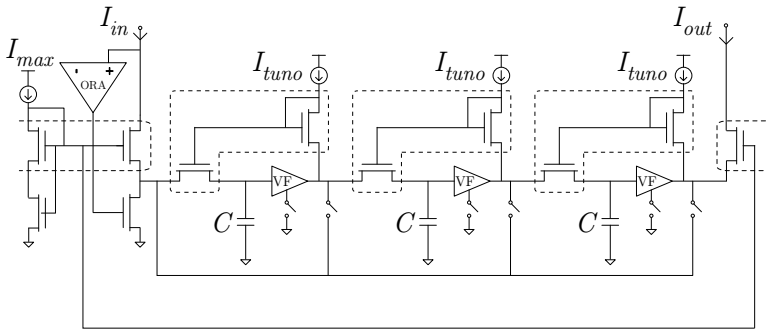


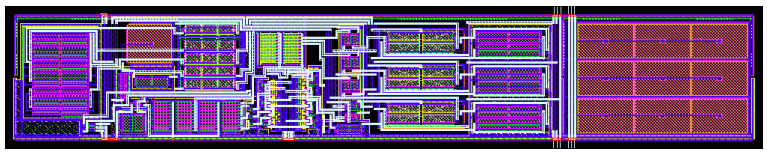
- Saturated GD 2nd-Order Band/Low-Pass:

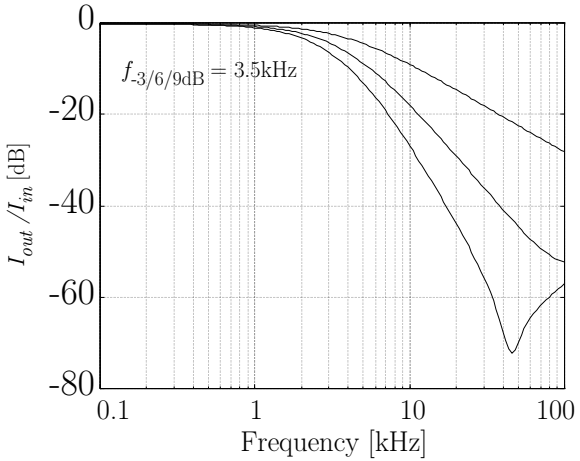


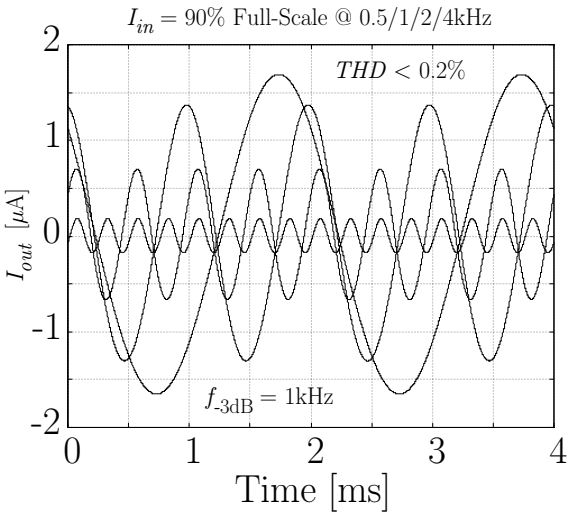


- Non-Saturated SD 3rd-Order Low-Pass:









- The MOSFET is suitable for Log-Companding Filtering
- Different types of CMOS Basic Building Blocks exist
- Importance of the design methodology to optimize filter area
- Compatibility with very Low-Voltage applications (e.g. Hearing Aids)

References

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